AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 52, lines 22-29 of the specification with the following amended paragraph (with strikethrough indicating deletions and underlining indicating additions):

-- Figure ~~P11~~ 39 is a schematic diagram of the scenario set forth in Figure **38** at cycle count 23 in accordance with an embodiment of the present invention. By cycle count 23, seven more bytes of packet 1 have been transferred into portion B **3804** of the input buffer 1. Also, as illustrated in Figure ~~P11~~ 39, in cycle count 23, memory access is allowed by the central controller and since portion A of input buffer 1 has been filled (since cycle count 16), the 16 bytes of data contained in portion A **3802** is read and written (see arrow ~~P1102~~ 3902) into memory bank 1 **3720** and then cleared from portion A **3802**.--